



- ★ Super Low Gate Charge
- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

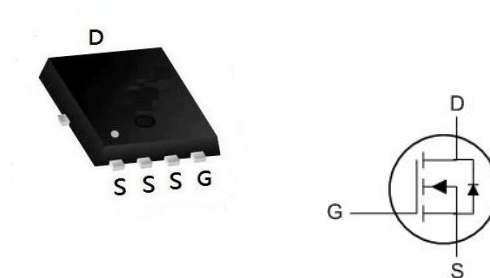
Product Summary

BVDSS	RDSON	ID
30V	3.5mΩ	100A

Description

The UD100N03D is the high cell density trench N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The UD100N03D meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

PDFN3333-8L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		10s	Steady State	
V_{DS}	Drain-Source Voltage	30		V
V_{GS}	Gate-Source Voltage	± 20		V
$I_D@T_C=25^\circ\text{C}$	Continuous Drain Current, $V_{GS}@ 10V^1$	100		A
$I_D@T_C=100^\circ\text{C}$	Continuous Drain Current, $V_{GS}@ 10V^1$	50		A
$I_D@T_A=25^\circ\text{C}$	Continuous Drain Current, $V_{GS}@ 10V^1$	30	19	A
$I_D@T_A=70^\circ\text{C}$	Continuous Drain Current, $V_{GS}@ 10V^1$	25	16	A
I_{DM}	Pulsed Drain Current ²	162		A
EAS	Single Pulse Avalanche Energy ³	144.7		mJ
I_{AS}	Avalanche Current	53.8		A
$P_D@T_C=25^\circ\text{C}$	Total Power Dissipation ⁴	62.5		W
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation ⁴	6	2.42	W
T_{STG}	Storage Temperature Range	-55 to 175		$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 175		$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	62	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹ ($t \leq 10s$)	---	25	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	2.4	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =30V, V _{GS} = 0V,	-	-	1.0	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±20V	-	-	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D =250μA	1.0	1.5	2.5	V
R _{DS(on)}	Static Drain-Source on-Resistance note3	V _{GS} =10V, I _D =30A	-	3.5	4.7	mΩ
		V _{GS} =4.5V, I _D =20A	-	6.0	10	
C _{iss}	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f = 1.0MHz	-	2100	-	pF
C _{oss}	Output Capacitance		-	326	-	pF
C _{rss}	Reverse Transfer Capacitance		-	282	-	pF
Q _g	Total Gate Charge	V _{DS} =15V, I _D =30A, V _{GS} =10V	-	45	-	nC
Q _{gs}	Gate-Source Charge		-	3	-	nC
Q _{gd}	Gate-Drain(“Miller”) Charge		-	15	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =15V, I _D =30A, R _{GEN} =3Ω, V _{GS} =10V	-	21	-	ns
t _r	Turn-on Rise Time		-	32	-	ns
t _{d(off)}	Turn-off Delay Time		-	59	-	ns
t _f	Turn-off Fall Time		-	34	-	ns
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	50	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	200	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _S =30A	-	-	1.2	V
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=100A/μs	-	15	-	ns
Q _{rr}	Body Diode Reverse Recovery Charge		-	4	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: T_J=25°C, V_G=10V, R_G=25Ω, L=0.5mH, I_{AS}=18.4A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%



Figure 1: Output Characteristics

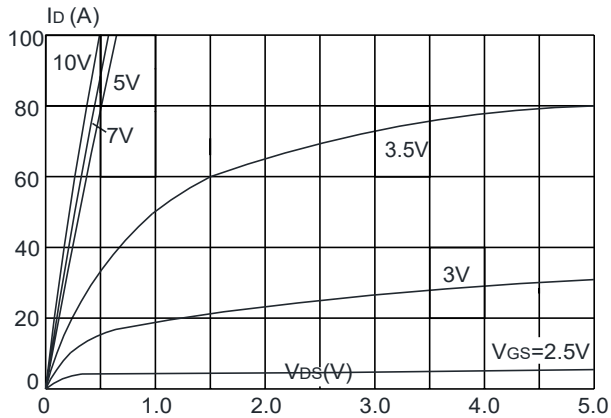


Figure 2: Typical Transfer Characteristics

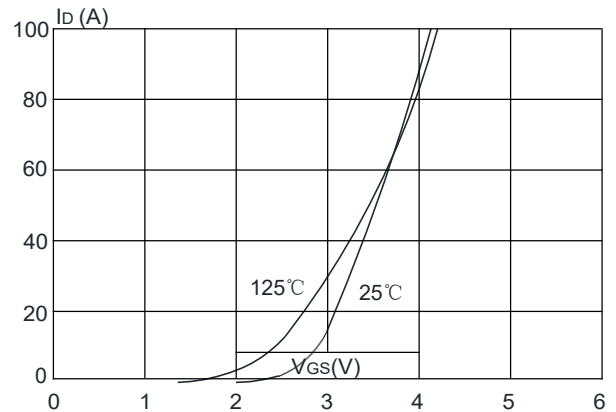


Figure 3: On-resistance vs. Drain Current

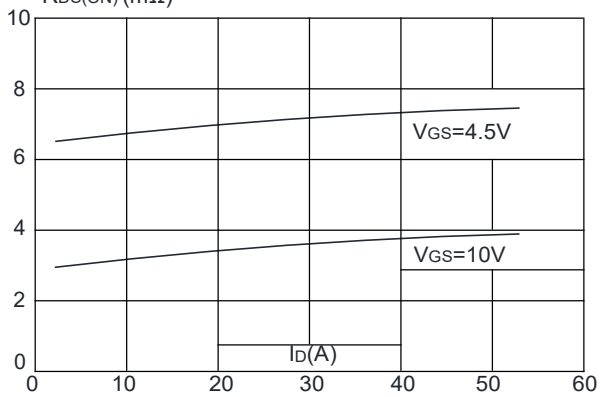


Figure 4: Body Diode Characteristics

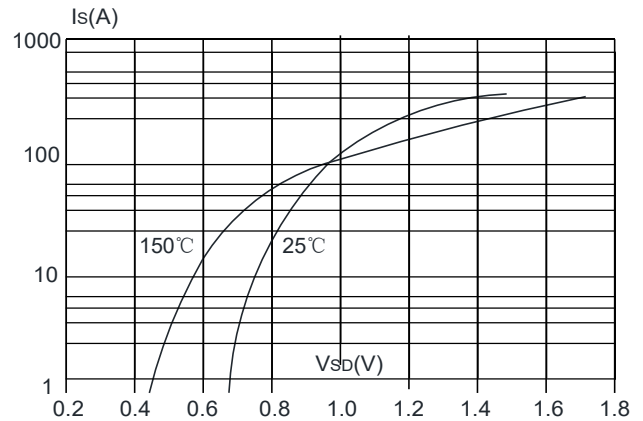


Figure 5: Gate Charge Characteristics

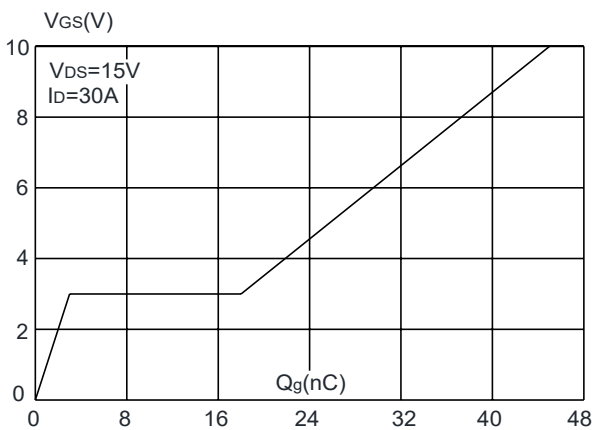


Figure 6: Capacitance Characteristics

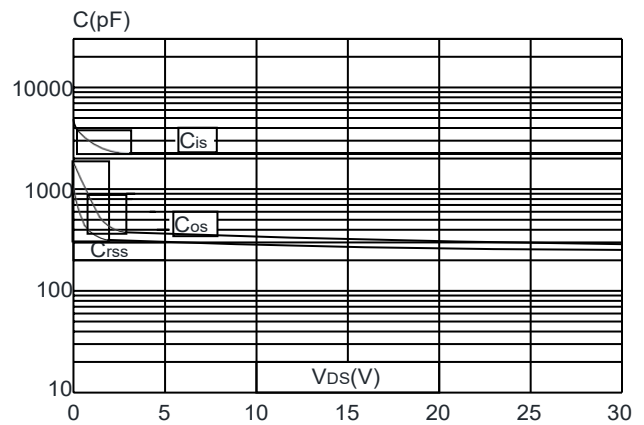




Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

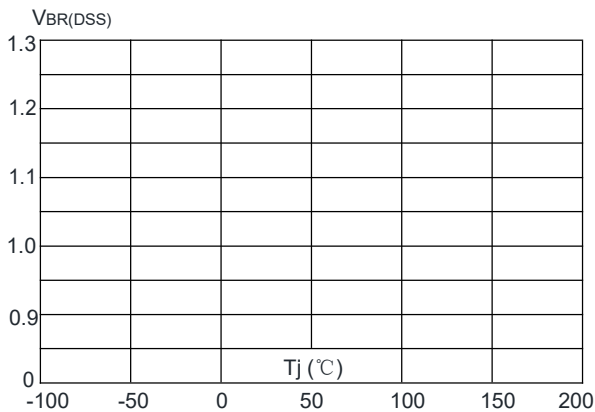


Figure 9: Maximum Safe Operating Area

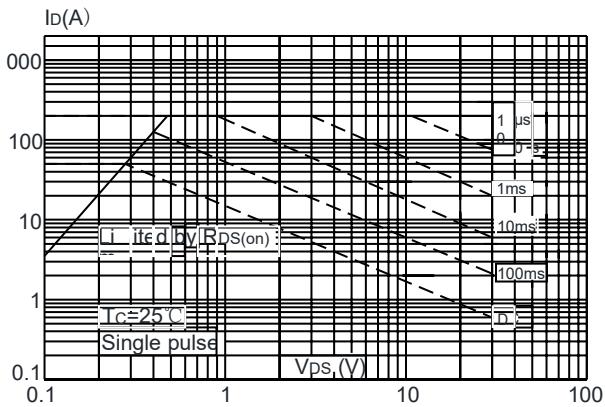


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case (PDFN3.3*3.3-8L)

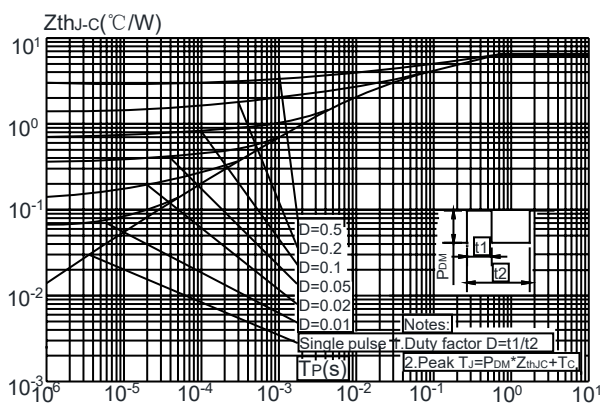


Figure 8: Normalized on Resistance vs. Junction Temperature

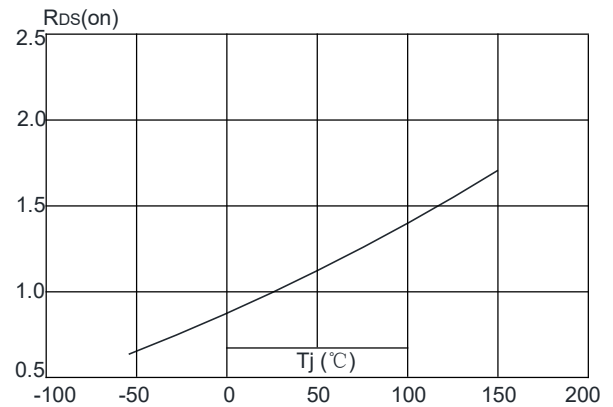
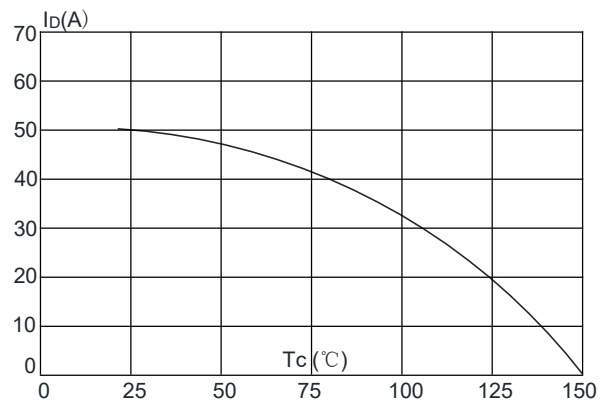


Figure 10: Maximum Continuous Drain Current vs. Case Temperature





Test Circuit

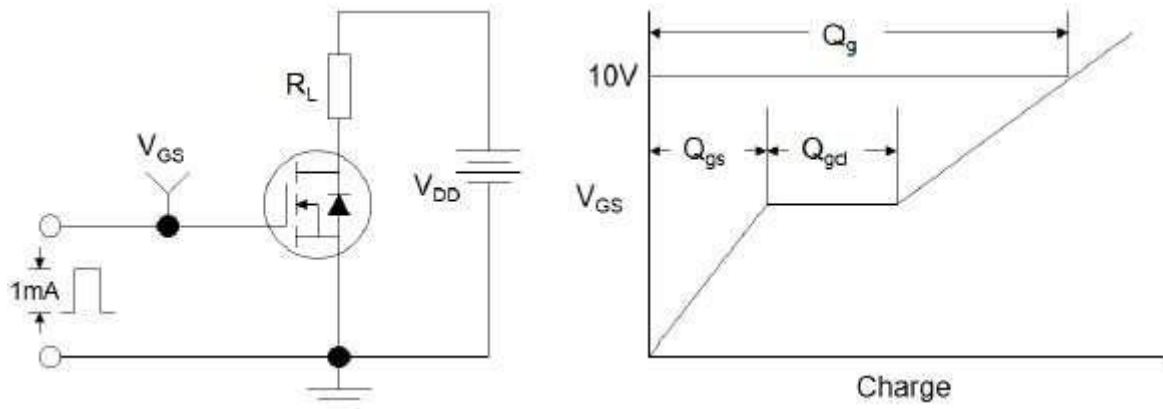


Figure1:Gate Charge Test Circuit & Waveform

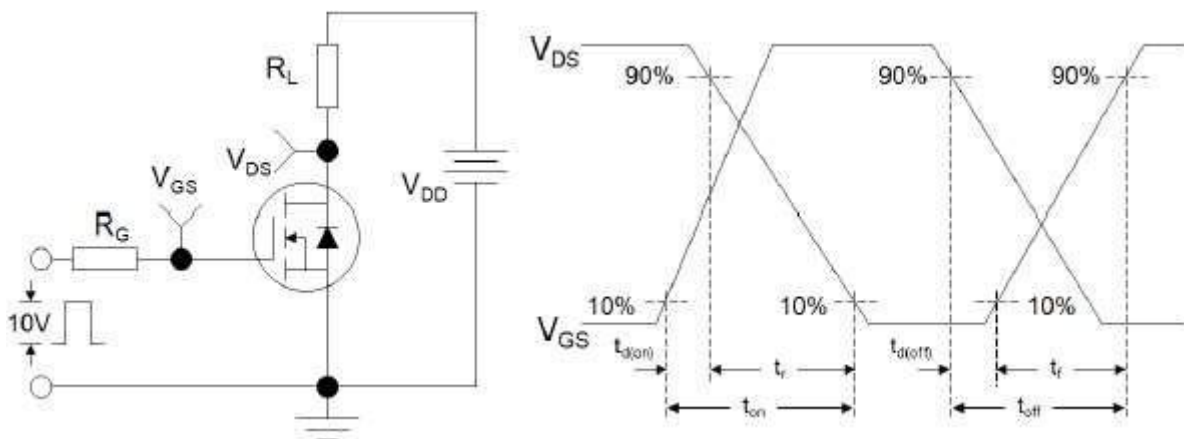


Figure 2: Resistive Switching Test Circuit & Waveforms

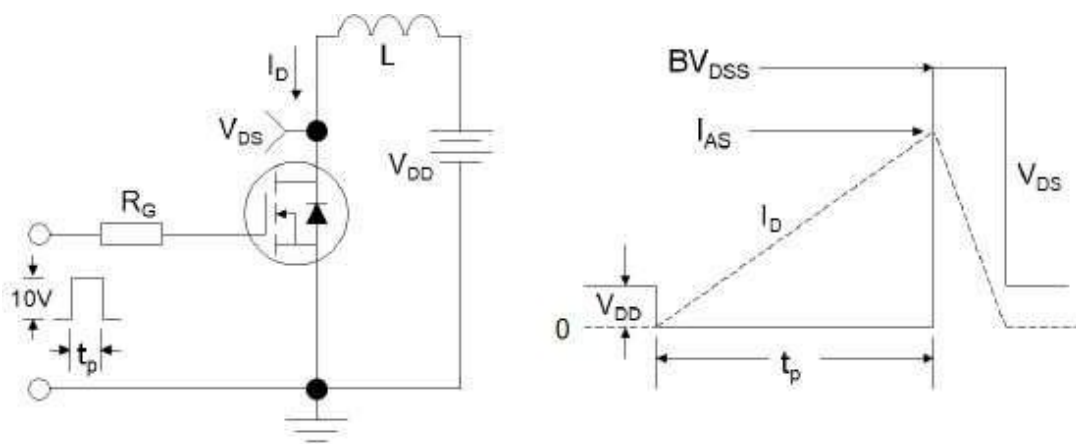
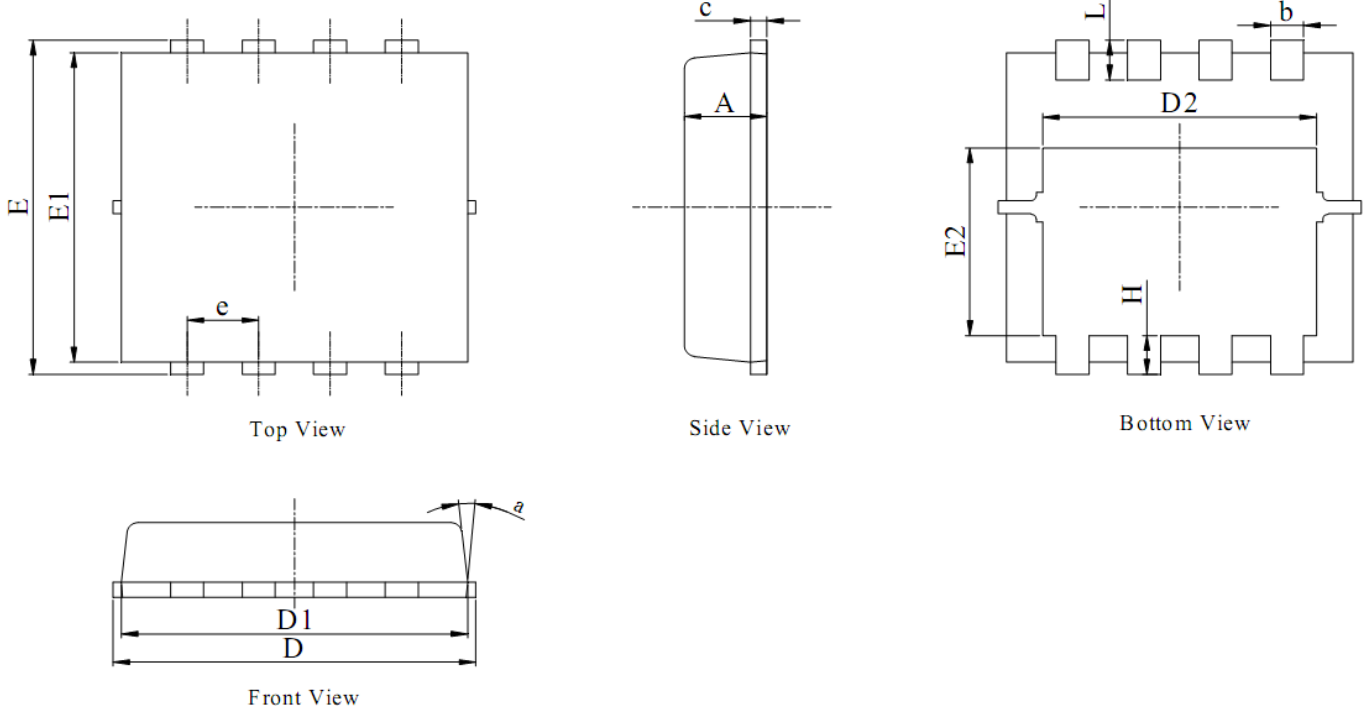


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



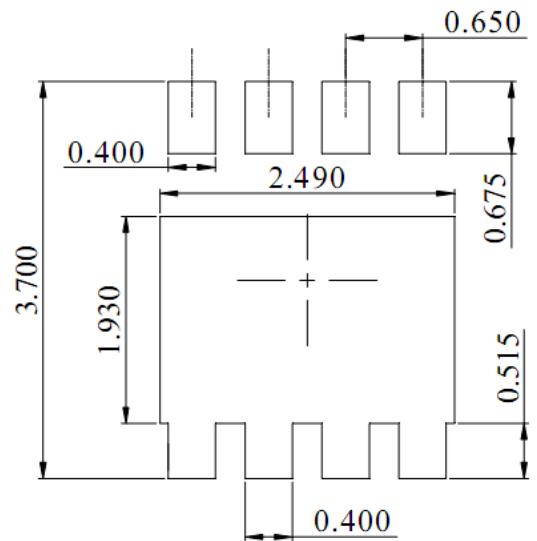
Package Mechanical Data-PDFN3333-8L-Single



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M,1994.
2. ALL DIMENSIONS IN MILLIMETER (ANGLE IN DEGREE).
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.20	0.25
D	3.00	3.15	3.25
D1	2.95	3.05	3.15
D2	2.39	2.49	2.59
E	3.20	3.30	3.40
E1	2.95	3.05	3.15
E2	1.70	1.80	1.90
e	0.65 BSC		
H	0.30	0.40	0.50
L	0.25	0.40	0.50
a	---	---	15°



DIMENSIONS:MILLIMETERS